This listing of the claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A method comprising:

providing a substrate comprising a first transistor structure comprising an n-type gate material and second transistor structure comprising a p-type gate material;

selectively removing the n-type gate material to form a recess in the first gate structure, wherein both the n-type gate material and the p-type gate material are exposed to the selective removal process; and

filling the recess with an n-type metal gate material.

2. (Original) The method of claim 1 wherein providing a substrate comprising a first transistor structure comprising an n-type gate material and second transistor structure comprising a p-type gate material comprises providing a substrate comprising an NMOS transistor structure comprising an n doped polysilicon gate material and a PMOS transistor structure comprising a p doped polysilicon gate material.

3. (Original) The method of claim 2 wherein providing a substrate comprising an NMOS transistor structure comprising an n doped polysilicon gate material

and a PMOS transistor structure comprising a p doped polysilicon gate material comprises providing a substrate comprising an NMOS transistor structure comprising an n doped polysilicon gate material and a PMOS transistor structure comprising a p doped polysilicon gate, wherein the PMOS transistor structure comprises source and drain regions comprising a silicon germanium alloy.

4. (Original) The method of claim 1 wherein selectively removing the n-type gate material comprises selectively removing the n-type gate material by wet etching the n-type gate material with a mixture of about 2 percent to about 30 percent ammonium hydroxide in deionized water and applying a sonication from about 0.5 MHz to about 1.2 MHz.

5. (Original) The method of claim 4 wherein wet etching the n-type gate material with a mixture of about 10 percent to about 20 percent ammonium hydroxide in deionized water comprises wet etching the n-type gate material with a mixture of about 10 percent to about 20 percent ammonium hydroxide in deionized water at a temperature from about 10 degrees to about 40 degrees Celsius.

6. (Original) The method of claim 1 wherein selectively removing the n-type gate material comprises wet etching the n-type gate material with a mixture of about 15 percent to about 30 percent tetramethylammonium hydroxide in deionized

water and applying a sonication from about 0.8 MHz to about 1.2 MHz.

7. (Original) The method of claim 6 wherein wet etching the n-type gate material with a mixture of about 15 percent to about 30 percent tetramethylammonium hydroxide in deionized water comprises wet etching the n-type gate material with a mixture of about 15 percent to about 30 percent tetramethylammonium hydroxide in deionized water at a temperature from about 60 degrees to about 90 degrees Celsius.

8. (Original) The method of claim 1 wherein selectively removing the n-type gate material comprises selectively removing the n-type gate material and not substantially removing the p-type gate material.

9. (Original) The method of claim 1 wherein selectively removing the n-type gate material to form a recess in the first gate structure further comprises selectively removing a first gate dielectric layer disposed beneath the n-type gate material.

10. (Original) The method of claim 9 wherein selectively removing the first gate dielectric layer disposed beneath the n-type gate material further comprises forming a second gate dielectric layer within the recess.

11. (Original) The method of claim 10 wherein forming the second gate dielectric layer within the recess comprises forming a high k gate dielectric layer within the recess.

12. (Original) The method of claim 10 wherein selectively removing a first gate dielectric layer disposed beneath the n-type gate material further comprises forming a high k gate dielectric layer selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide and combinations thereof within the recess.

13. (Original) The method of claim 1 wherein filling the recess with an n-type metal gate material comprises filling the recess with a metal gate material selected from the group consisting of hafnium, zirconium, titanium, tantalum, and aluminum.

14. (Currently amended) A method of forming a microelectronic structure comprising;

providing a substrate comprising an n-type transistor structure comprising an n-type polysilicon gate material and a p-type transistor structure comprising a p-type polysilicon gate material, wherein a first dielectric layer is disposed above the n-type and the p-type gate structures;

removing a portion of the first dielectric layer so that the n-type

polysilicon gate material is exposed;

selectively removing the n-type polysilicon gate material to form a recess, wherein both the n-type gate material and the p-type gate material are exposed to the selective removal process; and

filling the recess with an n-type metal gate material.

15. (Original) The method of claim 14 wherein filling the recess with an n- type metal gate material further comprises forming a second dielectric layer on the n-type metal gate material.

16. (Original) The method of claim 14 wherein selectively removing the n-type polysilicon gate material comprises selectively removing the n-type polysilicon gate material and not substantially removing the p-type polysilicon gate material.

17. (Original) The method of claim 14 wherein selectively removing the n-type polysilicon gate material comprises selectively removing the n-type gate material by wet etching the n-type gate material with a mixture of about 2 percent to about 30 percent ammonium hydroxide in deionized water and applying a sonication from about 0.5 MHz to about 1.2 MHz.

Claims 18-21 (Canceled).